

Final FA report of SY8824CAIC

Prepared by Silergy Corp.

CSIM-202209015

2022/10/13

Background



Part Number	SY8824CAIC	Package Type	TSOT23-8(FC)	Top Mark	UrDSA	Failure Source	massProduction		
Customer	Foxconn(ALT)	Application	Soundbar	Case Happenning Date	2022-08-26	Failure Rate	Failure Qty	TTL Production Qty	Failure Rate (ppm)
							1	315	0.3%

➤ Problem Description: No Power

➤ Part Number: SY8824CAIC

➤ Package Type: TSOT23-8(FC)

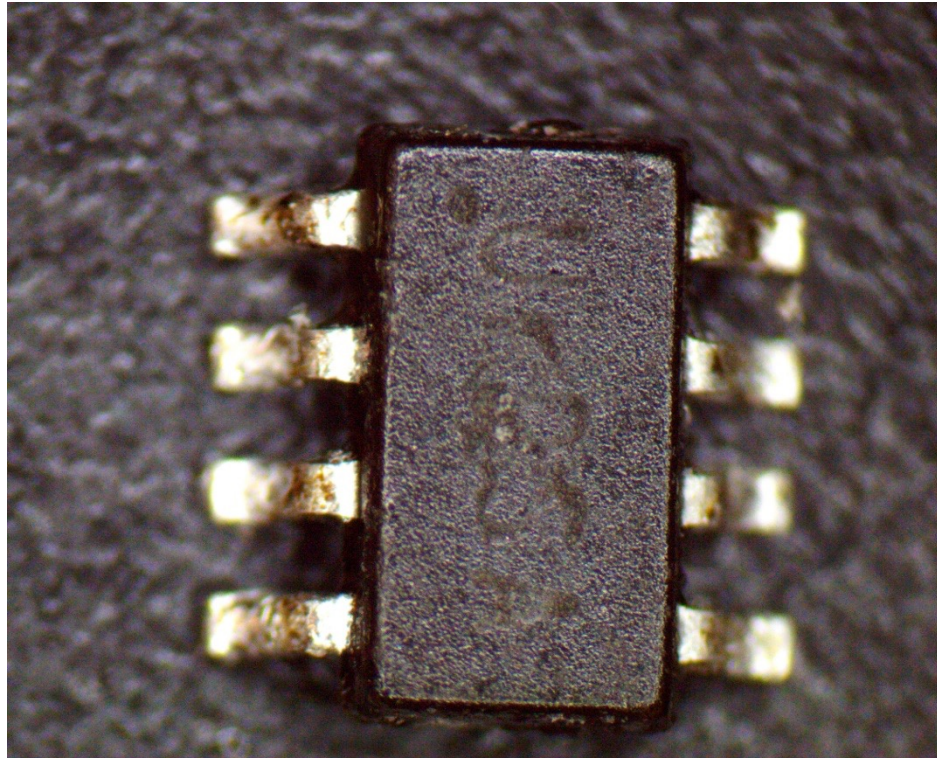
➤ Top Mark: **UrDSA**

➤ Failure Rate: $1/315=0.3\%$

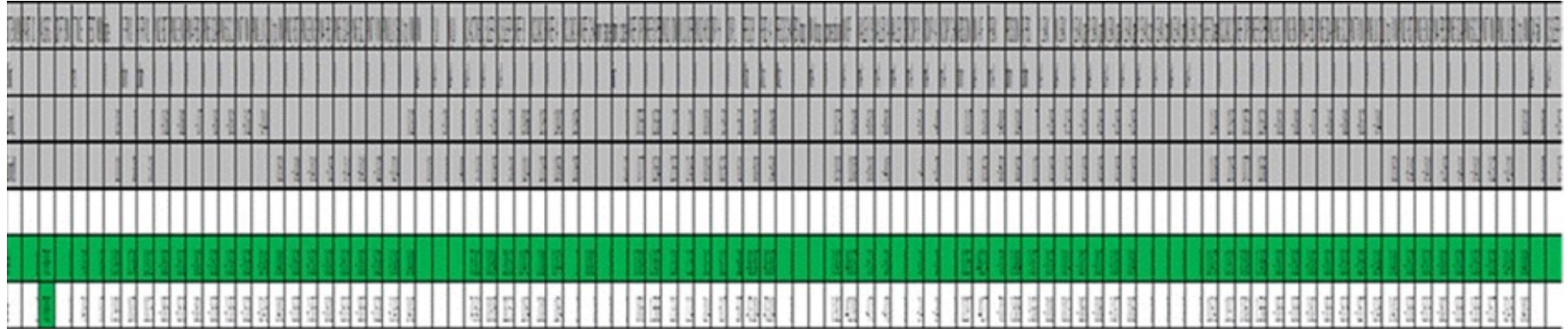
➤ Received Sample Qty:1 pcs

➤ Received Date: Sep 05th, 2022

Visual Inspection



➤ No abnormal was found at the top surface of package.



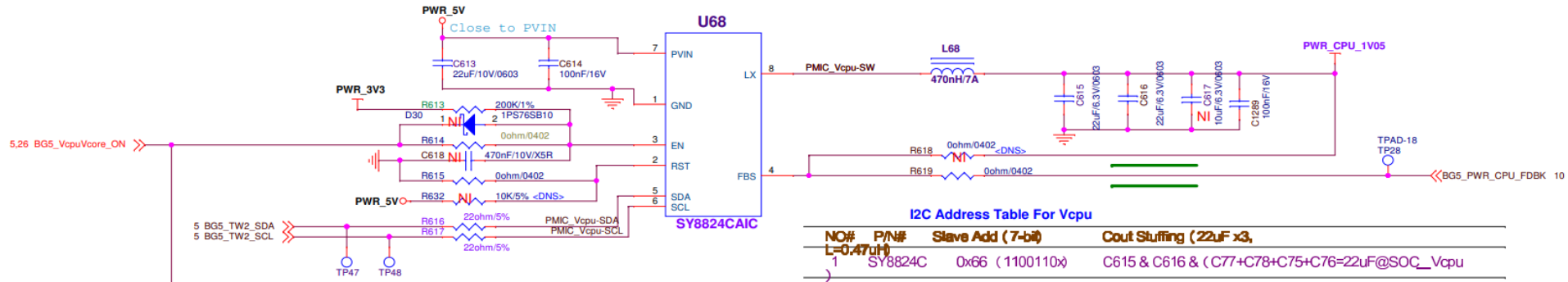
Silergy Corp. Confidential



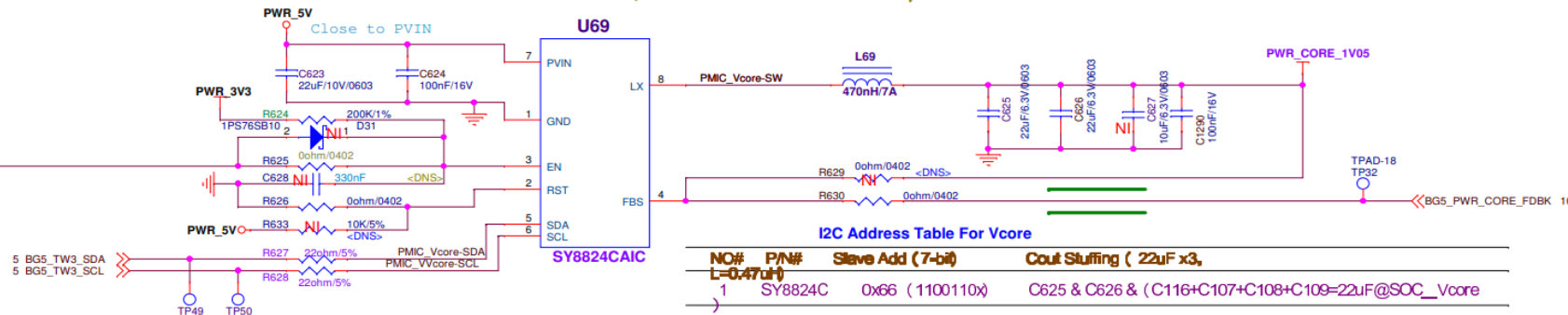
Bench Test



Default 1.05V/4A for Vcpu;

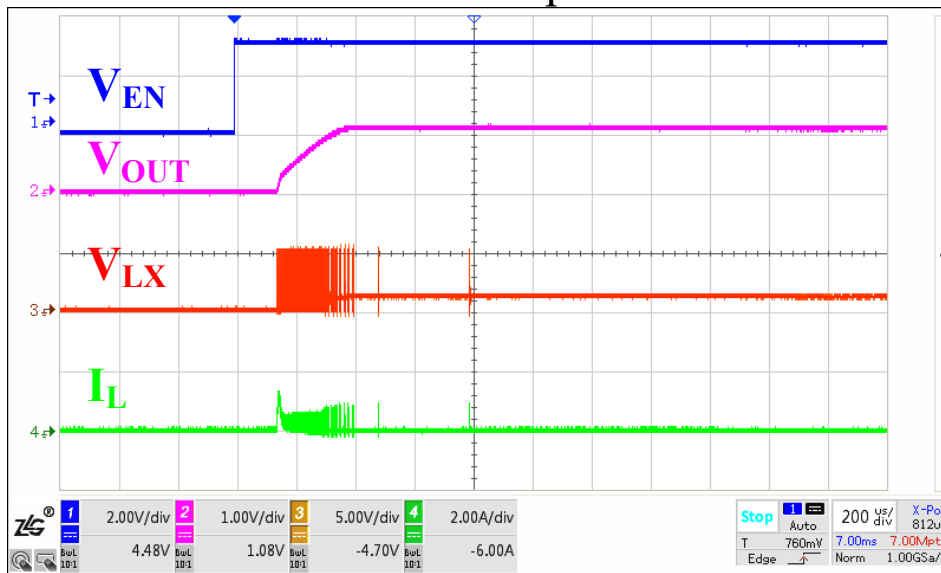


Default 1.05V/4A for Vcore;



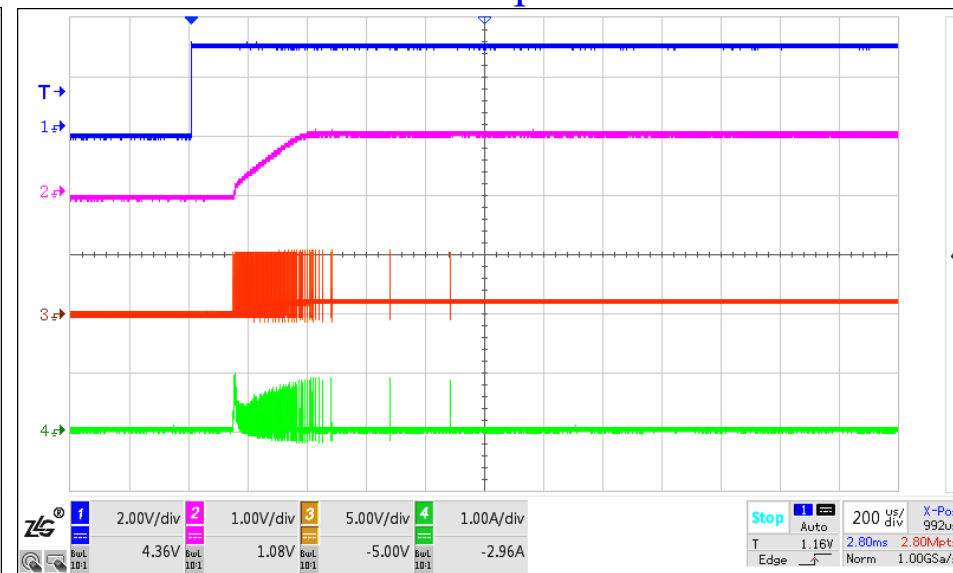


Ref Chip



$I_{OUT}=0A$

FA Chip#1

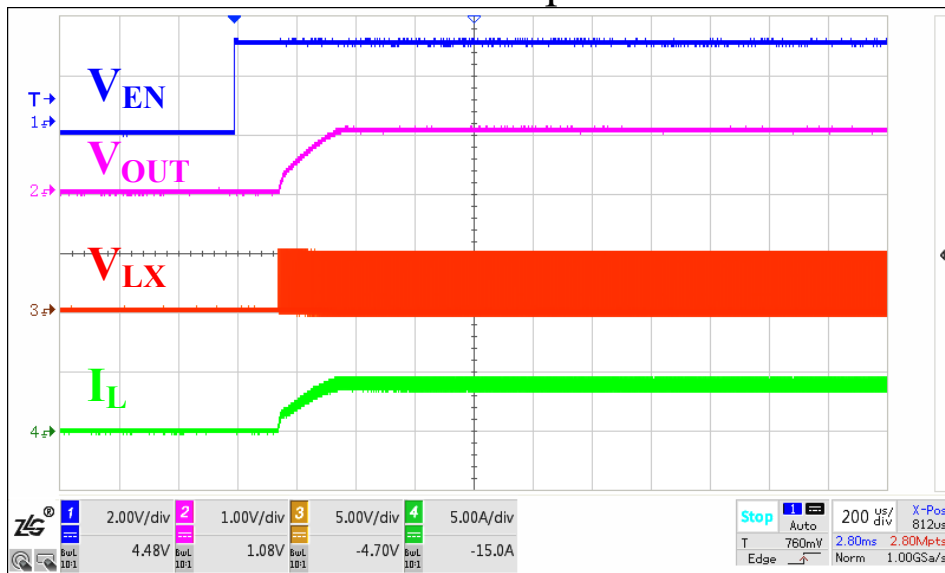


OK

$I_{OUT}=0A$

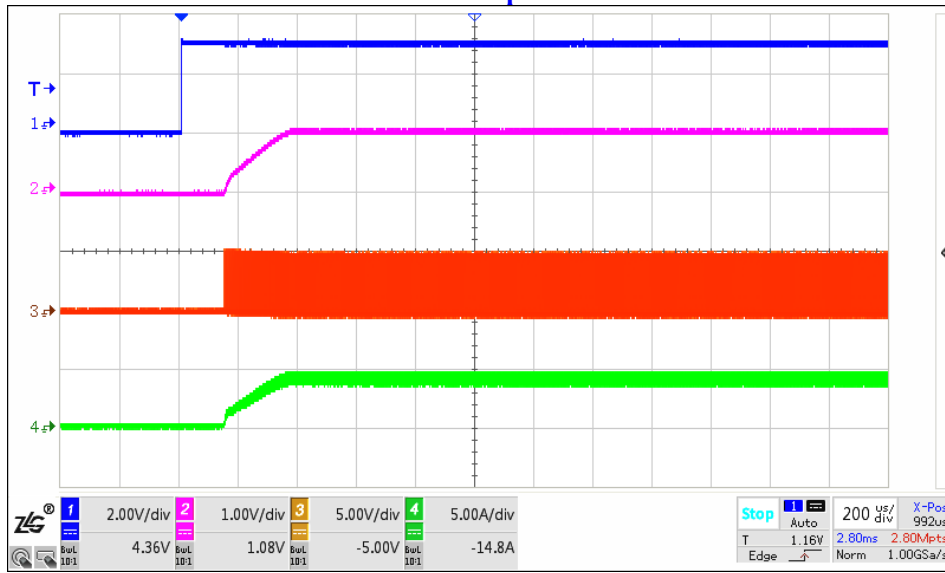


Ref Chip



$I_{OUT}=4A$

FA Chip#1

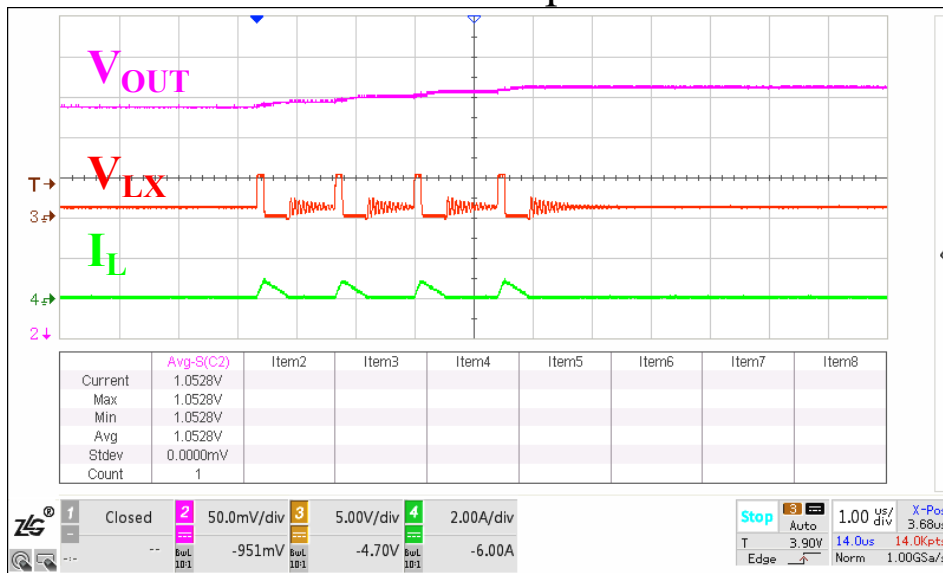


OK

$I_{OUT}=4A$

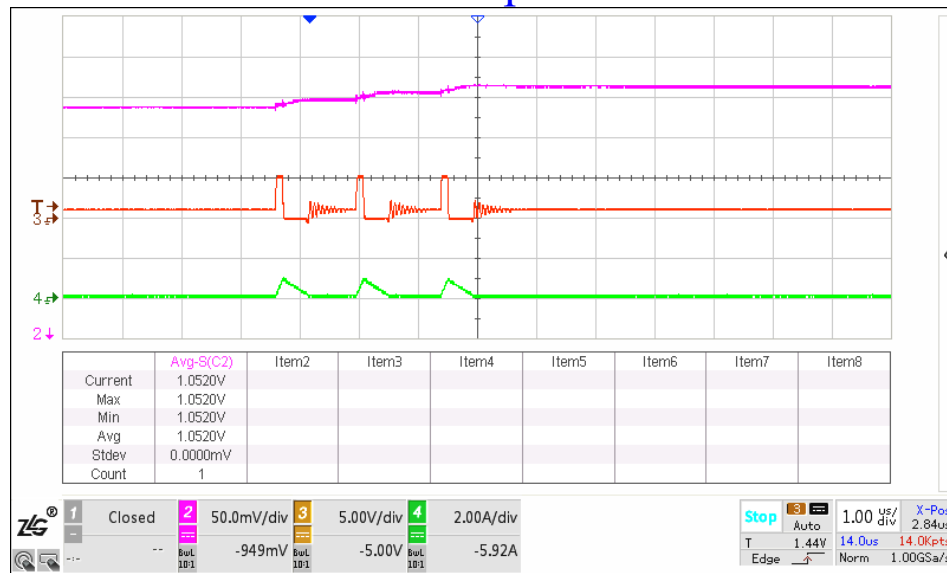


Ref Chip



$I_{OUT}=0A$

FA Chip#1



OK

$I_{OUT}=0A$



Ref Chip



$I_{OUT}=4A$

FA Chip#1



OK

$I_{OUT}=4A$



Quiescent Current/Shutdown Current Test

Quiescent Current I_Q Test Condition:

$$V_{IN}=V_{EN}=5.0V, I_{OUT}=0A, V_{FB}=105\%V_{REF}.$$

$V_{IN}(V)$ $I_Q(uA)$	FA Chip	#Ref	#1
5.0		68.4	67.7

#1's quiescent current is OK.

Shutdown Current I_{SHDN} Test Condition:

$$V_{IN}=5.5V, V_{EN}=0.$$

FA Chip	#Ref	#1
$I_{SHDN}(uA)$	0.1	<0.1

#1's shutdown current is OK.

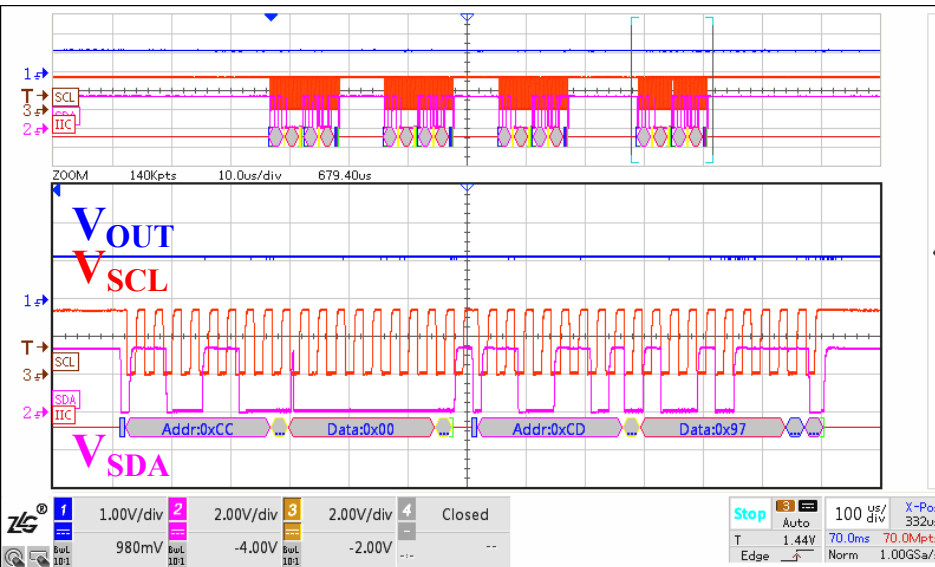


	Set Value: 10000000			Set Value: 10010111			Set Value: 10111111		
	Write	Read	Vout(V)	Write	Read	Vout(V)	Write	Read	Vout(V)
#Ref	0x80	0x80	0.764	0x97	0x97	1.049	0xBF	0xBF	1.548
#1	0x80	0x01	0.767	0x97	0x17	1.055	0xBF	0x3F	1.558

#1's I2C read function is fail.

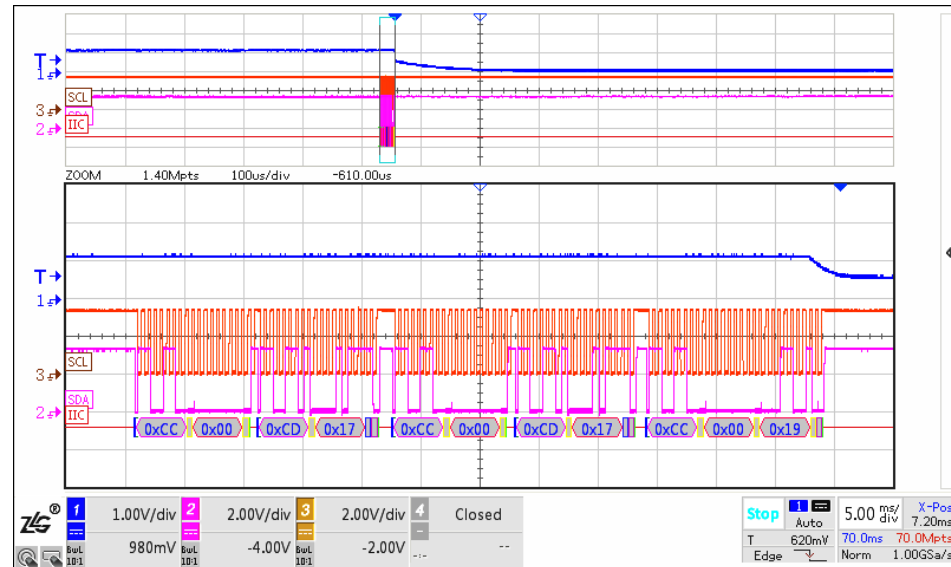


Ref Chip



Read Data: 0x97, OK.

FA Chip#1



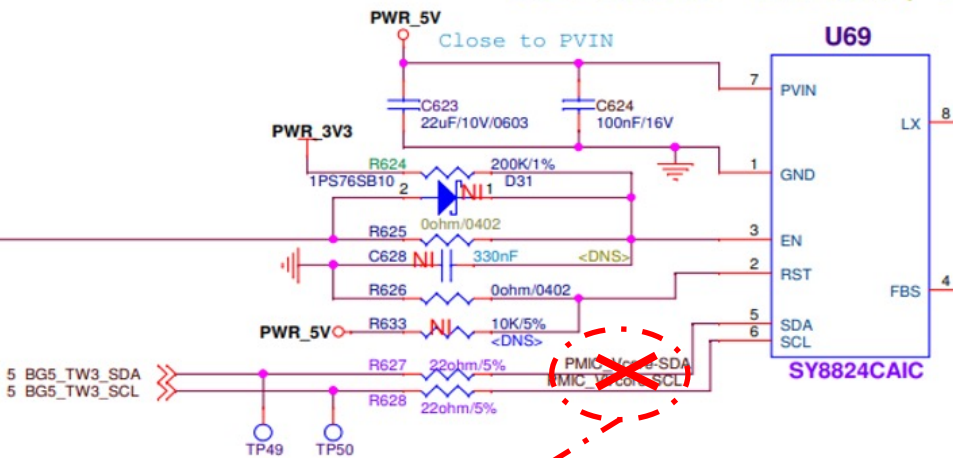
Read Data: 0x17, wrong;
Write Data:0x19, Buck_EN OFF, IC shutdown.

For FA chip #1, I2C master wrote a data 0x19, which makes IC soft-ware shutdown.

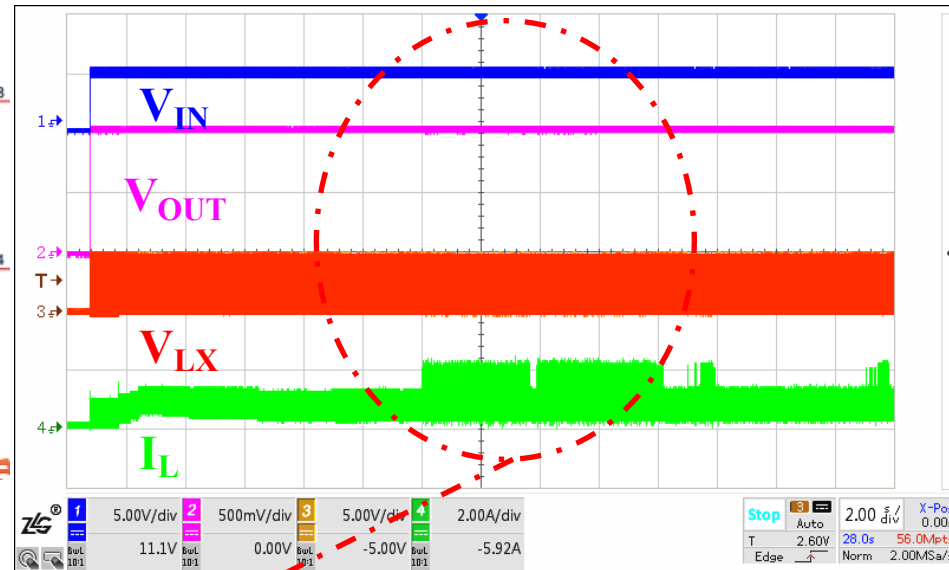


FA Chip#1

Default 1.05V/4



Cut the wire of SDA to prevent transfer path from I2C master to SY8824C.



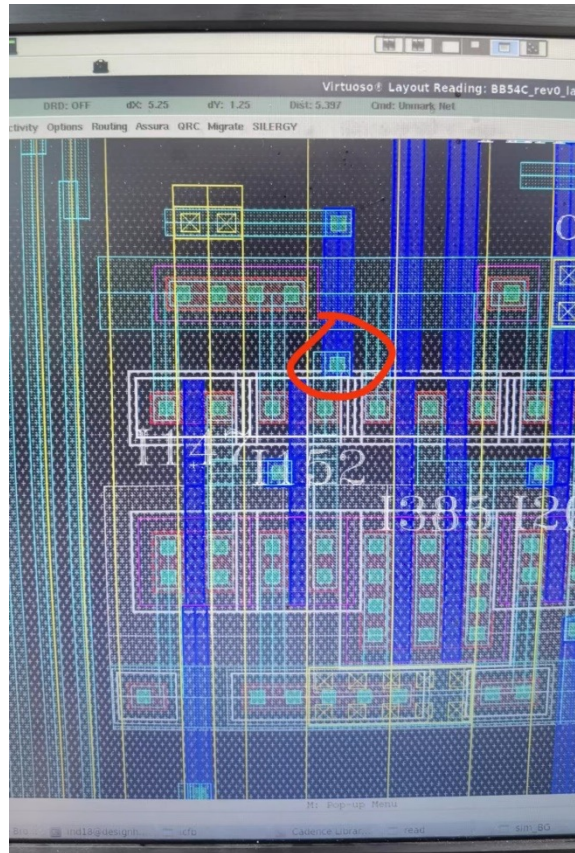
If cutting off the wire of SAD, SY8824C will not shutdown.



Bench Summary

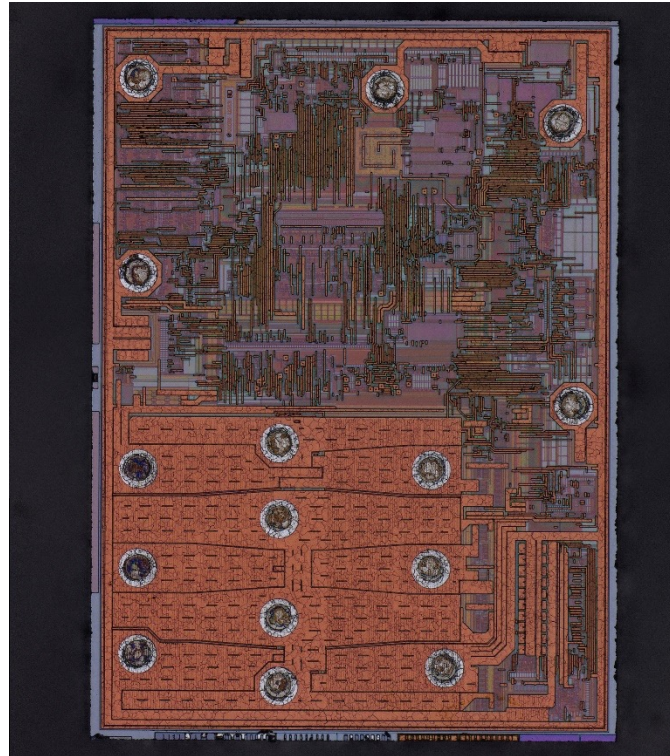
➤ Returned #1 I2C read function was failed on Bench Test

Possible Root Cause



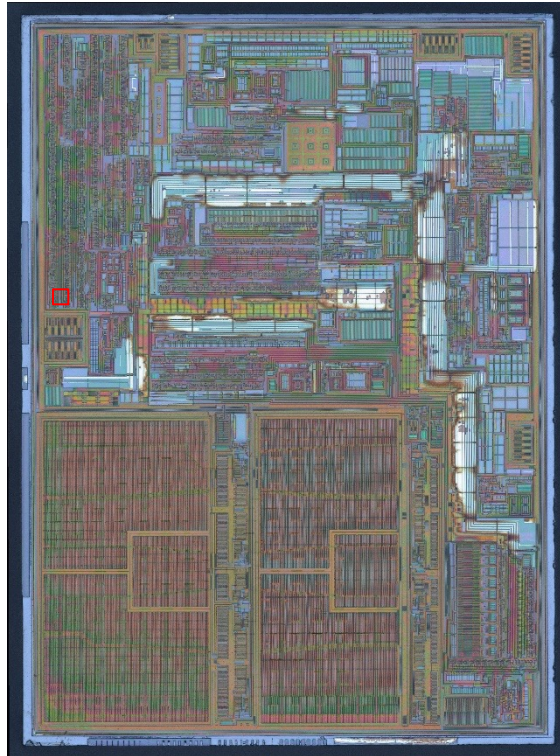
➤Returned #1 I₁₅₂ 下拉增大, delay增强, 导致 read function 错误。

Decap



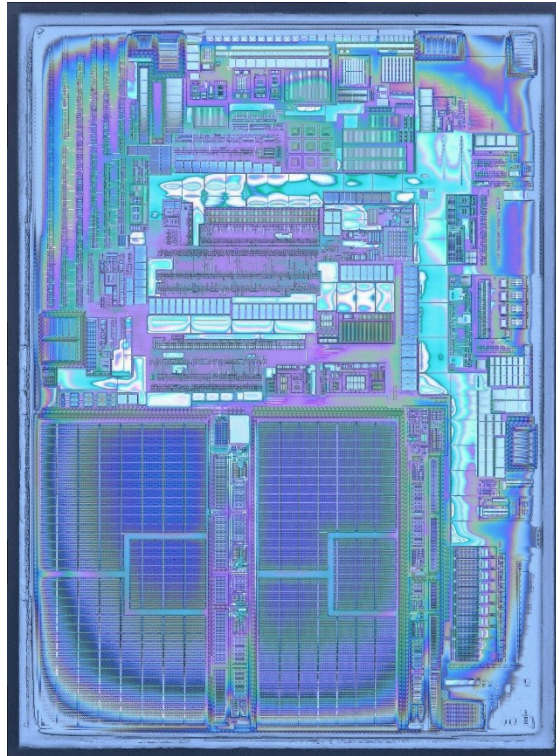
➤ No abnormal were found on die surface after Decap.

Delayer-M1



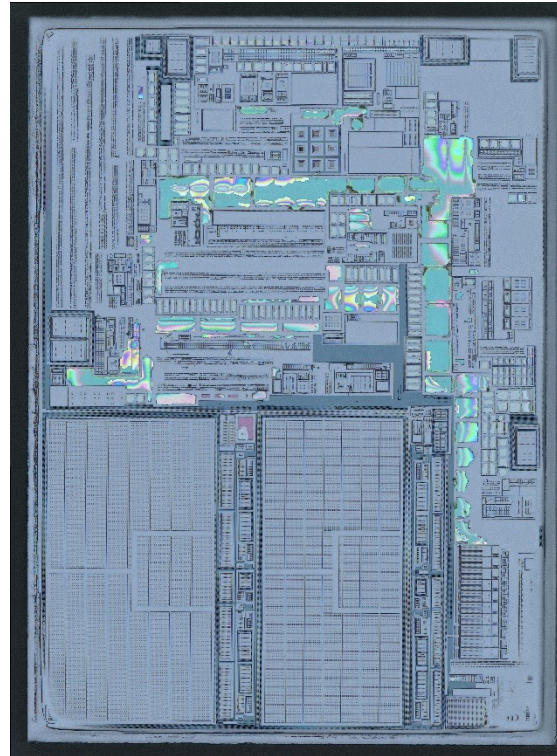
➤ No abnormal were found on die surface after Delayer.

Delayer-CT



- No abnormal were found on die surface after Delayer.

Delayer-SUB



➤ No abnormal were found on die surface after Delayer.



FA Summary



From above analysis, returned #1 was damaged by EOS event, but the damage was too small to be observed directly by Delayer .

- EOS let IC internal circuit (I152) get damage and 12C read function abnormal (base on page 12~16's analysis).
- Silergy also add the test program to verify read/write function to filter the suspect product which may damage in our production line.
(material with date-code 2236 been tested by new program)



Thank you!